## REMARKS

Reconsideration of this application as amended is respectfully requested. Claims 1-43 were presented for examination. Claims 1-5, 19, 20, 26, 27, 30-33 and 38 were rejected. Claims 6-18, 21-25, 28, 29, 34-37 and 39-43 were objected to. Claims 1, 5, 6, 7, 10, 15, 16, 17, 18, 26, 40, 41 and 43 have been amended. Claims 1-43 are presented for examination.

***Statement of Substance of Interview with the Examiner***

On Tuesday, May 8, 2007, a telephonic interview was conducted between Ronald Shea, attorney for the Applicant, and United States Patent Examiner Pierre-Michel Bataille. Figure 12 of the application was referenced for background, discussing the nature of a single command packet to address multiple memory devices in a memory chain. Claim 1 was discussed in view of U. S. Patent Application 09/893,616 to Greff (hereinafter "Greff,") and U.S. Patent Application No. 10/215,719 to Eatherton (hereinafter "Eatherton.") Counsel for Applicant noted that neither Greff nor Eatherton disclose or suggest a memory controller configured to transmit an access command that selects two or more memory devices. Applicant proposed amending the phrase "and that selects" to "wherein the memory access command selects" to clarify that the two or more memory devices are identified in a single command. The Examiner indicated he would examine further the Greff and Eatherton references to see of either of these references disclose a memory chain with a memory controller configured to address two or more memory devices in a single command.

***Rejections Under 35 U.S.C. § 102***

Claims 1-5, 19-20, 26-27, 30-33 and 38 have been rejected under 35 U.S.C. 102(b) as anticipated by Greff is directed to a point-to-point bus operation that includes a

memory controller 31 linked a series of memory modules 24, 26 by a segmented bus. (Greff Title, Figure 1 and paragraph 0031). The problems addressed by Greff are stubs that create signal reflections (Greff, paragraph 0005) and overloading a bus with multiple memory devices that create capacitive drain on the bus (Greff, paragraph 0006), thereby slowing down the operational speed. The focus of Greff is to disconnect unused bus portions by switching operations, thereby allowing the bus to function as a point-to-point communication path (Greff, Abstract).

The segmented data bus may be a multi-drop bus (Greff, paragraph 0032). Within each memory module coupled to the bus is an interface circuit 30 (Greff, Figs. 1, 2, 3) that is able to isolate some of the memory modules from the controller means of a field effect transistor (FET switch 39), (Greff, Figures 2, 3 and paragraph 0036), thereby lightening the capacitive load on the network. Additionally, interface circuit 30 within each memory module 24, 26 (Greff, Figures 1-3) is able to selectively transmit or decoupled data from the bus 24 to memory devices 54, 56, 58, 60 served through a particular interface circuit 30 of a particular memory module 24. (See Greff, Figures 4 & 5 and paragraph 0056).

Paragraph 3, page 3 of the Office Action noted that Greff "shows a memory controller connected to the memory chain to select the memory device to be accessed, the memory device consisting of a set of two or more memory devices." Applicant does not acknowledge that the trunk-line architecture of Greff depicts a "chain." However, assuming, arguendo, that the trunk-line architecture of Greff can be understood as a "chain," Greff simply does not disclose a memory controller configured to generate or transmit ***memory access commands for accessing multiple memory devices by a single command***. Moreover, Greff does not disclose circuitry that would even be capable of buffering or processing a single command directing access to multiple memory devices. Therefore, such a feature is not even *suggested* by Greff.

In contrast to the teachings of Greff, the referenced application (the "Application") discloses a memory system having a plurality of memory devices coupled to one another in a chain, with a first memory device coupled to a memory controller. ***The controller is configured to output a memory access command that selects a set of two or more of the memory devices to be selected by that command.*** (Application, abstract.) It is important to note that this is not accomplished by a sequence of separate commands, but to a single command. This feature is conceptually illustrated, inter alia, in Figure 9, element 203, which discloses a "short form command packet" and Figure 10, element 220, which discloses a "long form command packet." (Application, paragraph 0065, lines 1-2). Thus, the long-form command packets 220 are used to convey *read and write commands and other* ***commands that specify address values or ranges of address values within the target memory devices***. (Application, paragraph 0067, last 5 lines). Figure 12 of the Application illustrates an embodiment wherein memory controller 151 is coupled to input commands to a chain of memory devices beginning with MEM 1 which is coupled in a chain with MEM 2, and so forth to MEM 8 which is coupled back to the memory controller. In the example of Figure 12, memory devices MEM 4 through MEM 6 are targeted by the command packet 231. Following this command, a stream of data is sent along the memory chain without further commands specifying which memory module is to store the data. This has been accomplished by a single command.

Claim 1 recites, in part,

> a plurality of memory devices coupled one to another in a chain, including a first memory device and a last memory device;
>
> a memory controller coupled to the first memory device in the chain, the memory controller configured to output a memory access command to the first memory device in the chain, ***wherein the memory access command selects a set of two or more of the memory devices to be accessed***.

Greff does not directed in any manner to the nature of command packets

transmitted along the Greff network. Accordingly, Greff does not disclose or suggest a "*memory controller configured to output a memory access command to the first memory device in the chain,* ***wherein the memory access command selects a set of two or more of the memory devices to be accessed,"*** as recited in claim 1. In view of this clear distinction, Greff does not teach or disclose every element of Claim 1, and therefore does not anticipate independent Claim 1. For at least these reasons, independent Claim 1 and claims 2-5 and 19-20, which depend therefrom, stand allowable over the teachings of Greff.

Claim 26 recites:

> A method of operation in a memory controller, the method comprising:
> receiving a memory access request; and
> outputting a memory access command to a plurality of memory devices coupled one to another in a chain, the ***memory access command including selection information to select two or more of the memory devices to be accessed.***

Applicant respectfully submits that, for reasons stated above in conjunction with Claim 1, Claim 26 is also not anticipated by Greff. Greff simply does not teach anything about the method or apparatus for outputting a memory access command. Accordingly, Greff does not disclose or suggest anything about a ***memory access command including selection information to select two or more of the memory devices to be accessed***, as recited in claim 26. In view of this clear distinction, Greff does not teach or suggest every element of claim 26, and therefore, does not anticipate Claim 26. For at least these independent Claim 26, and claims 27, 20-33 and 38 which depend therefrom, stand allowable over Greff.

Claims 1-5, 19-20, 26-27, 30-33 and 38 have been rejected under 35 U.S.C. §

102(b) as anticipated by Eatherton. Paragraph 0030 of Eatherton recites, "As shown each progressive stage forwards error messages to a next associative memory stage or to control logic." In chain transmission, commands, data, error checks, and other transmissions are received by one member of the chain, and actively transmitted to the member. Applicant therefore agrees that the language of Eatherton in paragraph 0030 is consistent with chain-architecture known in the prior art. Eatherton recites a chain transmission of an error message. However, Eatherton does not disclose or suggest a method or apparatus for transmitting a memory access command over chain-type architecture wherein ***a single memory access command selects two or more memory devices to be accessed***.

In contrast to the teachings of Eatherton, Claim 1 recites, in part,

> a plurality of memory devices coupled one to another in a chain, including a first memory device and a last memory device;
>
> a memory controller coupled to the first memory device in the chain, the memory controller configured to output a memory access command to the first memory device in the chain, ***wherein the memory access command selects a set of two or more of the memory devices to be accessed***.

For reasons discussed above, applicant submits that Eatherton does not disclose or suggest a memory controller configured to output a memory access command to the first memory device in the chain, ***wherein the memory access command selects a set of two or more of the memory devices to be accessed***, as recited in independent Claim 1. In view of this clear distinction, Eatherton does not teach or disclose every element of Claim 1, and therefore does not anticipate independent Claim 1. For at least these reasons, independent Claim 1 and claims 2-5 and 19-20,

which depend therefrom, stand allowable over the teachings of Eatherton.

Claim 26 recites:

> A method of operation in a memory controller, the method comprising:
> receiving a memory access request; and
> outputting a memory access command to a plurality of memory devices coupled one to another in a chain, the ***memory access command including selection information to select two or more of the memory devices to be accessed.***

Applicant respectfully submits that, for reasons stated above in conjunction with Claim 1, Eatherton does not disclose or suggest every element of Claim 26 either, and therefore, does not anticipate Claim 26. For at least these reasons, independent Claim 26, and claims 27, 30-33 and 38 which depend therefrom, stand allowable over Eatherton.

***Allowable Subject Matter***

Claims 6-18, 21-25, 28-29, 24-27 and 39-43 have been objected to as being dependent on a rejected base claim, but have been deemed allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Applicant acknowledges the allowability of claims 6-18, 21-25, 28-29, 24-27 and 39-43, but in view of the foregoing remarks, respectfully declines to rewrite claims 6-18, 21-25, 28-29, 24-27 and 39-43 in independent form at this time.

***Petition for Extension of Time***

Applicant hereby enters a request for extension of time in the filing the foregoing reply by a period of two (2) months under the provisions of 37 CFR 1.136(a). Applicant

claims small entity status. Payment in the amount of $225 is tendered herewith electronically. If electronic submission of payment is unsuccessful, payment will be tendered to the PTO by FAX or First Class Mail within 24 hours of failure of submission of electronic payment.

***Conclusion***

Applicant submits that all claims are in condition for allowance, and requests notification of allowance at the earliest available opportunity. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Respectfully submitted,

LAW OFFICES OF RONALD R. SHEA

Date May 10, 2007

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